UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,087	04/02/2004	Hung C. Lin	MSI-7	9474

7590 07/05/2006

HungChang Lin
8 Schindler Ct.
Silver Spring, MD 20903

EXAMINER	
LE, LANA N	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 07/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,087	LIN ET AL.	
	Examiner	Art Unit	
	Lana N. Le	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-2,5-15 is/are rejected.

7)☒ Claim(s) 3-4 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-6, 8-11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin et al (US 6,735,422).

Regarding claim 1, Baldwin et al disclose a DC offset compensation system for a direct conversion receiver (fig. 5), comprising:

an incoming radio frequency signal (RsubRF);

an inherent local oscillator signal from oscillator 229 (fig. 2) with a frequency equal to that of the incoming frequency signal;

at least one mixer (301) to mix the radio frequency signal with the local oscillator signal to generate a zero frequency intermediate frequency (IF) signal;

a double sampling means having a calibration phase (401) and a signal flow phase (303,305,307,313) wherein a compensation signal is generated and stored during the calibration phase (401), and the IF signal is processed during the signal flow phase (processing of IF signal 303, 305,307,313);

means (401) to generate and store any DC offset (within LUT 501) of the IF signal as the compensating signal during the calibration phase (401) (col 19, lines 35-53); and

means to insert the compensating signal (injecting DC compensating signal via 329, 325, 297 and 307) in the IF signal to cancel the DC offset of the IF signal during the signal flow phase (col 18, lines 30-46; col 19, lines 32-53).

Regarding claim 5, Baldwin et al disclose the DC offset compensation system as described in claim 1, wherein the calibration signal is applied to the input of the radio receiver (201 via 297) during the calibration phase (fig. 5).

Regarding claim 6, Baldwin et al disclose the DC offset compensation system as described in claim 1, further comprising a low noise amplifier (LNA portion of 301) at the input of the receiver before the mixer (col 14, lines 61-67).

Regarding claim 8, Baldwin et al disclose the DC offset compensation system as described in claim 1, wherein the calibration signal (PGM) is applied at the output of the mixer (after mixer 301 at block 307) (fig. 5).

Regarding claim 9, Baldwin et al disclose the DC offset compensation system as described in claim 1, wherein the calibration signal is a DC voltage (col 18, lines 30-34; col 19, lines 21-25, fig. 4).

Regarding claim 10, Baldwin et al disclose the DC offset compensation system as described in claim 9, wherein the DC voltage is zero (col 18, lines 30-34, fig. 4).

Regarding claim 11, Baldwin et al disclose the DC offset compensation system as described in claim 1, wherein the calibration signal is an AC calibration signal without

superimposed DC voltage, and a low-pass filter is used to remove the AC component of the calibration signal (col 12, lines 55-58).

Regarding claim 14, Baldwin et al disclose DC offset compensation system as described in claim 1, wherein the system also compensates for 1/f noise in the IF signal (col 12, lines 29-54).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin et al in view of Pai et al (US 2005/0,118,980).

Regarding claim 2, Baldwin et al disclose the DC offset compensation system as described in claim 1, wherein the compensation signal is generated by applying a calibration signal (calibration signal from 401) to derive the compensating signal and storing the compensating signal (col 19, lines 32-53). Baldwin et al do not disclose storing the DC offset across a capacitor. Pai et al disclose storing the DC offset across a capacitor (para. 7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to store the DC offset on a capacitor in order to be able cancel the offset easily by discharging the capacitor.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin et al in view of Lindskog et al (US 7,039,016).

Regarding claim 7, Baldwin et al disclose the DC offset compensation system as described in claim 6, wherein Baldwin et al do not disclose the calibration signal is applied before the mixer. Lindskog et al a calibration signal is applied before the mixer (fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to calibrate before the mixer in order to allow the mixer to shift the frequency of the calibrated signal so that the calibration can be done across different narrow frequency bands.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin et al (US 6,735,422) in view of Seppinen et al (US 2003/0,176,174)

Regarding claim 12, Baldwin et al disclose the DC offset compensation system as described in claim 11, wherein Baldwin et al do not disclose the calibration signal has the same frequency as the LO signal. Seppinen et al disclose the calibration signal has the same frequency as the LO signal (para. 54, 57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the calibration signal has the same frequency as the LO signal in order to reduce the need for an additional oscillator to simplify circuitry components as suggested by Seppinen et al.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin et al (US 6,735,422).

Regarding claim 13, Baldwin et al disclose the DC offset compensation system (fig. 5) as described in claim 1, wherein Baldwin et al in fig. 5 do not disclose the local

oscillator generates a in-phase LO signal and a quadrature LO signal, which mix with incoming RF signal in an in-phase mixer and a quadrature mixer, respectively, and to generate in-phase the IF signal and quadrature the IF signal, respectively. However, as is notoriously old in the art I, Q signals are generated in common ZIF transceiver as shown in Baldwin et al (fig. 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the mixer of fig. 5 include I and Q signals and I, Q LO signal in order to calibrate differential phase signals and to inject DC offset from the carrier frequencies generated by the LO which varies with channel selection to eliminate DC offsets from both the Q and Q channels within the ZIF transceiver (col 11, lines 47-57).

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin et al (US 6,735,422) in view of Hayashi et al (US 6,909,882).

Regarding claim 15, Baldwin et al disclose DC offset compensation system as described in claim 1, further Baldwin et al do not disclose comprising more than one the compensation signal applied to more than one stage of the IF amplifier. Hayashi et al disclose more than one the compensation signal (from 117) applied to more than one stage of the IF amplifier (115) (fig. 4) (col 2, lines 64-67; col 8, lines 7-53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to calibrate more than one amplifier in order to compare outputs of the amplifiers with reference voltages in successive approximation to apply the proper voltages to the amplifiers to cancel the DC offset based on the comparison results as suggested by Hayashi et al (col 8, lines 26-53).

Allowable Subject Matter

8. Claims 3-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 3, Baldwin et al disclose the DC offset compensation system as described in claim 2, wherein Baldwin et al and the cited prior art fail to disclose the compensating signal is derived by applying the calibrating signal to the non-inverting input terminal of an operational amplifier, short-circuiting the output of the operational amplifier to the inverting terminal of the operational amplifier to derive the compensating signal at the inverting terminal of the operational amplifier, and wherein the compensating signal is stored in a capacitor with first electrode connected to the inverting terminal and second electrode of the capacitor connected to ground.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N. Le whose telephone number is (571) 272-7891. The examiner can normally be reached on M-F 9:30-18:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on (571) 272-7899. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lana Le

6-19-06

LANA LE
PRIMARY EXAMINER